REMARKS

The foregoing amendments, and the following remarks, are deemed fully responsive to the pending office action of June 29, 2004. Claims 1-10, 13-18 are amended, without new matter, to clarify that the requests are memory access requests, as supported throughout the specification of the '971 Application.

The disclosure is objected to because the Examiner states that an application serial no. is missing on page 14, line 2. However, the '971 Application has only 7 pages, 2 pages of claims and two pages of drawings. Further clarification of this objection is requested. A review of the specification of the '971 Application also does not indicate a missing serial number, as stated by the Examiner.

Moreover, the Examiner states in the Office Action Summary that the current office action is responsive to communications of June 26, 2001; however, the '971 Application was filed on October 26, 2001, which is after the noted communication. Clarification is also requested as to this summary comment.

Claim Rejections – 35 U.S.C. § 101

Claims 1, 4, 5, 8, 11, 12, 14 and 16-19 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. With regard to claims 1, 4, 5, 8, 11, 12, 16-19, and as noted above, these claims are amended to denote that the requests are "memory access" requests within processing architecture (e.g., a CPU or chipset); such amendments ensure that the claims fall within 35 U.S.C. § 101. Reconsideration of claims 1, 4, 5, 8, 11, 12, 16-19 is thus requested.

As for claims 14, the term 'logic' is specifically defined within the '971 Application: "By way of example, the logic may be a CPU, chipset, bus controller, switch or other logic handling the request." See '971 Application, page 7, lines 1 and 2. The CPU, chipset, bus controller and switch are, for example, electronic circuitry that implements the logical functions. The 'logic' may for example include electronic circuit gates of such circuitry. Applicant thus believes that the claims are sufficiently supported. Note for example that amended claim 14 recites a CPU architecture that initiates both speculative and non-speculative memory access requests, and requires the following elements:

a) decode logic for determining whether the memory access requests are speculative,

b) assessment logic for determining one or both of interconnect and target resource conditions,

c) the CPU architecture processing speculative memory access requests, or not, as a function of the conditions.

The 'decode logic' thus decodes the memory access requests to determine whether they are speculative, and the 'assessment logic' thus assesses one or both of interconnect and target resource conditions. An "interconnect," as described by the '971 Application, can be a bus, a crossbar, a switch, or a point-to-point protocol. The assessment logic may thereby monitor conditions of busses, crossbars, switches and point-to-point protocols. Reconsideration of claim 14 is thus requested.

Claim Objections

Claim 2 and claim 3 are objected to because the term 'first identifier' was mentioned in claim 1. Claim 2 is amended to use the term 'the first identifier'. Claim 3 depends from claim 2 and therefore objections to both claims 2 and 3 are corrected. Reconsideration is requested.

Claim Rejections – 35 U.S.C. § 112

Claims 14, 15 and 17 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the immediate invention. Claim 14 is amended to remove the phrase 'of the type', and to replace 'the' improvement' with 'an' improvement, to attend to the Examiner's rejection. Claim 15 depends from claim 14 and benefits from like argument.

Claim 17 is also slightly amended to attend to the Examiner's rejections.

Accordingly, it is believed that amended claims 14, 16 and 17 comply with 35 U.S.C. §112. Reconsideration is requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,567,901 issued to Neufeld (hereinafter "Neufeld'901"). Respectfully, Applicant disagrees.

To anticipate a claim, Neufeld'901 must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F2.d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Neufeld'901 does not teach every element of claims 1-19.

Neufeld'901 discloses a system with read around speculative load. However, in the system of Neufeld'901, the decision to cancel a request, or to upgrade speculative requests to non-speculative, is made by the processor, and depends upon the execution path of the processor through software. For example, Neufeld'901 discloses (see col 5, lines 60-62): '...the processor 30 might pause the application 451 and issue another memory request 421 to shorten the delay.' Similarly, Neufeld'901 further discloses (see col 5 lines 65-67, col 6 lines 1-2): 'If the processor 30 reaches a point where it realizes that it is not going to need memory request 421, the processor 30 would generate a memory request indicating that the memory request 421 may be cancelled. The Neufeld'901 processor thus determines and initiates the modification of the status of memory requests. Neufeld'901 does not describe a system whereby one or both of interconnect and target resource conditions are used to determine if a speculative memory request is processed, or not, as in each independent claim (claims 1, 14 and 16) of the '971 Application.

More particularly, the '971 Application teaches a system that handles speculative memory access requests (e.g., memory access requests that are predicted by prefetch unit 26 of processor 12, for example). The '971 Application also teaches additional logic circuitry that assesses the condition of the interconnect (e.g., a bus connecting a processor to a memory device) and a target resource (e.g., a memory device) to determine if a speculative memory access will be processed, delayed or aborted. See the '971 Application, e.g., page 3, paragraph 11.

Accordingly, amended claim 1 recites a method for processing a memory access request within a processing architecture, and requires the steps of:

a) determining whether the memory access request is speculative or not based upon a first identifier;

b) assessing one or both of interconnect and target resource conditions in the event that the memory access request is speculative; and

c) either processing the memory access request, or not, as a function of the conditions.

In step b), claim 1 specifically requires that one or both of the interconnect and target resource conditions is assessed to determine if a speculative memory access request is processed. Neufeld'901 does not teach or suggest this feature, at least, and therefore cannot anticipate claim 1. Moreover, Neufeld'901 specifically recites (col. 5, line 65 – col. 6, line 2) that the processor "...realizes that it is not going to need a memory request 421, the processor 30 would generate a memory request indicating that the memory request 421 may be cancelled." Thus, in Neufeld'901, a speculative request 421 may only be cancelled by the processor 30, whereas, in the '971 Application, the assessment logic may abort a speculative memory access if resource conditions so dictate.

The Examiner argues that the memory request processing logic of Neufeld'901 assesses (or checks) the target resource condition in order to complete the speculative memory request 421. However, this assessment is by protocol, and does not determine if 'traffic on bus 30 is too congested' or that 'target memory ... is saturated' - as in the '971 Application. Such a protocol does not therefore include decision logic that may postpone or abort processing of a speculative memory request.

Accordingly, reconsideration and allowance of claim 1 are requested.

Claims 2 through 13 depend from claim 1, and benefit from like arguments. Specifically, the arguments hereinabove clearly show that Neufeld'901 does not teach each and every element of claim 1 and that, therefore, Neufeld'901 cannot also teach the elements of claims 2-13. But in the context of claim 1, these claims have additional reasons for patentability. Note for example the following features of claims 2-9.

- Amended claim 2 recites decoding the first identifier as a first bit field within the memory access request.
- Amended claim 3 recites encoding the first bit field within the memory access request to define a speculative ID of the memory access request.
- Amended claim 4 recites that the memory access request includes one of an instruction, a message and an operational request.
- Amended claim 5 recites determining a priority of the memory access request based upon a second identifier, in the event that the memory access request is speculative, and processing the memory access request, or not, based upon the conditions and the priority.
- Amended claim 6 recites determining a priority by decoding the second identifier as a second bit field within the memory access request.
- Amended claim 7 recites encoding the second bit field within the memory access request to define a priority of the memory access request.
- Amended claim 8 recites that the memory access request includes one of a memory read request and a memory load request.
- Amended claim 9 recites utilizing one of a CPU, chipset and memory controller to determine whether the memory access request is speculative.

In addition, note that amended claim 10 recites that at least one of the CPU, chipset and memory controller independently controls the step of processing the memory access request based on the conditions. Neufeld'901 does not teach of processing the memory access request based on such conditions. Neufeld'901 discloses that a system prioritizes requests, giving priority to non-speculative requests; but it does not teach that conditions (traffic and congestion) of the interconnect and the target resource are used during processing of a memory access request. Neufeld'901 also does not consider bus traffic and target resource congestion. The use of a communication protocol on a bus cannot reasonably anticipate the assessment of bus traffic conditions or target resource congestion as described in the '971

Application. In Neufeld'901, processor 30 modifies the status of a speculative request based upon execution of the application 451. See Neufeld'901, col. 5, lines 56-62, and col. 5 line 65 through col. 6 line 2. Accordingly, Neufeld'901 does not, and cannot, teach every element of claim 10.

Claim 11 recites that the step of assessing target resource conditions includes assessing one or more of memory utilization, memory congestion, buffer space utilization, and bus congestion. Claim 12 recites that the step of assessing interconnect conditions includes assessing one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization. As noted above, Neufeld'901 does not teach of monitoring memory utilization, memory congestion, buffer space utilization or bus congestion. Accordingly, Neufeld'901 does not, again, anticipate claims 11, 12.

Amended claim 13 recites the step of notifying one or more logic devices when the memory access request is not processed. Accordingly, the determination of whether the memory access request is processed, or not, may be made external to the processor, wherein the processor is informed if the speculative memory access request is aborted.

Neufeld'901, on the other hand, discloses that the processor determines if a request is deleted, based upon algorithm execution. According to Neufeld'901, a first speculative request is issued to the memory controller, and, later, the processor may send a second request to inform the memory controller not to process the first speculative request. Unlike Neufeld'901, therefore, the determination to process or abort a speculative memory access request may be made by the memory controller, for example. If the memory controller determines that the speculative memory access request is to be aborted, the memory controller sends notification of the aborted speculative memory access request to the processor.

Claim 14 recites CPU architecture that initiates both speculative and non-speculative memory access requests, an improvement comprising decode logic for determining whether the memory access requests are speculative, and assessment logic for determining one or both of interconnect and target resource conditions, the CPU architecture processing speculative memory access requests, or not, as a function of the conditions. The assessment logic of claim 14 may therefore assess the condition

of the interconnect or target resource. As argued above, Neufeld'901 does not teach utilizing conditions of the interconnect or target resource. Neufeld'901 also teaches away from the present inventions (in each independent claim) in that it is the processor that generates instructions to change the status of, or to delete, speculative requests. See Neufeld'901, col. 5, lines 56-67, col. 6, lines 1-2.

With regard to claim 14, the Examiner again contends that '...assessing target resource condition is an inherent step.' We respectfully disagrees. A bus protocol may utilize control signals to correctly sequence data transfer to and from a resource; however, such a protocol does not assess 'conditions' of the resource as required by claim 14. See also the '971 Application, paragraphs 12, 31 and 32. Accordingly, the assessment logic may determine if a speculative memory request will be processed, or not, based upon the 'condition' of the memory resource, independent of any decision by the processor. Accordingly, as in other claims, Neufeld'901 does not teach or suggest claim 14.

Claim 15 depends from claim 14 and benefits from like arguments.

Claim 16 recites a system for processing speculative memory access requests, comprising: one or more memory access requests having a bit field defining the memory access requests as speculative or non-speculative; decode logic for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic for processing speculative memory access requests, or not, based on at least one of interconnect and target resource conditions.

As previously argued above, Neufeld'901 does not teach or suggest processing logic for processing speculative requests, or not, based on at least one of interconnect and target resource conditions. We disagree, again, with the Examiner's statement that 'assessing target resource condition is an inherent step.' Moreover, unless these types of rejections are removed, we request evidence pursuant to MPEP §2144 that supports the Examiner's contention. We contend that assessing the target resource or the interconnect condition to determine if the target resource is saturated, or if the interconnect is congested [e.g., see the '971 Application, paragraph 31], is not inherent to processing speculative requests as disclosed by Neufeld'901.

Claims 17-19 depend from claim 16 and benefit from like arguments. But these claims have additional reasons for patentability. For example, in amended claim

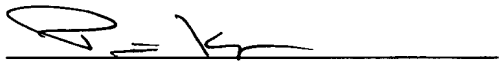
17, one or both of the decode logic and processing logic are located within a CPU, a chipset, a bus controller or a memory controller. Neufeld'901 simply does not teach or disclose such decode and processing logic.

Claim 19 recites a bus controller for assessing one or more of bus congestion and bus utilization conditions. Neufeld'901 does not teach assessing bus congestion and bus utilization conditions for purposes of determining if speculative requests are processed or not.

For the reasons discussed above, Applicant believes that amended claims 1-19 are not anticipated by Neufeld'901. Reconsideration and allowance of all claims are requested.

Applicants believe no fees are due in connection with this Amendment and Response; however, if any fee is deemed necessary, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

Peter C. Knops, Reg. No. 37,659
LATHROP & GAGE L.C.
2345 Grand Blvd., Suite 2400
Kansas City, MO 64108
Telephone: (816) 292-2000
Facsimile: (816) 292-2001